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ANNA UNIVERSITY (UNIVERSITY DEPARTMENTS)

B.E. /B.Tech / B. Arch (Arrear) - END SEMESTER EXAMINATIONS, NOV / DEC 2024

ELECTRONICS AND COMMUNICATION ENGINEERING

III Semester

EC5303 - DIGITAL SYSTEM DESIGN

(Regulation2019)

Time:3hrs Max.Marks: 100

CO1	Ability to apply Boolean algebra and simplification procedure to digital logic
CO2	Ability to design combinational digital circuits using logic gates
CO3	Ability to analyze and design synchronous sequential circuits
CO4	Ability to analyze and design synchronous sequential circuits
CO5	Ability to understand the working of logic gate electronic circuits and memory device

BL – Bloom's Taxonomy Levels

(L1-Remembering, L2-Understanding, L3-Applying, L4-Analysing, L5-Evaluating, L6-Creating)

PART- A(10x2=20Marks)

(Answer all Questions)

Q.No.	Questions	Marks	CO	BL
1	Given the two binary numbers X = 1010100 and Y = 1000011, perform the subtraction X – Y using 1's complement?	2	1	3
2	Converting the following number Hexadecimal to octal: $(4243)_{16}$?	2	1	3
3	Draw the 4-bit adder/subtractor with overflow detection structure?	2	2	4
4	Implement the NOT gate using 2 x1 MUX?	2	2	2
5	List out the types of triggering in flip-flop?	2	3	2
6	Distinguish between Moore and Mealy model?	2	3	1
7	Define critical and non-critical race?	2	4	1
8	What is Hazard in asynchronous sequential circuit?	2	4	2
9	What is BiCMOS?	2	5	1
10	What are the types of ROM in memory device?	2	5	2

PART- B(5x 13=65Marks)

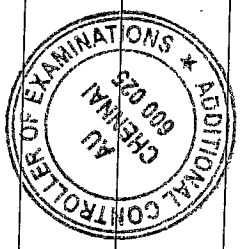
(Restrict to a maximum of 2 subdivisions)

Q.No.	Questions	Marks	CO	BL
11 (a)	(i) Express the Boolean Function F= A+B'C as a sum of minterms?	6	1	3
	(ii) Reduced the Boolean expression using K-Map F (A, B, C, D) =$\sum$m (2,5,7,9,11,12,14) + $\sum$d (3,4,6).	7		
	OR			

11 (b)	Simplify the following Boolean function using Quine-McClukey tabular method? $F(A,B,C,D)=\sum m(2,6,8,9,10,11,14,15)$	**13**		
12 (a)	(i) Obtain design equations for a Binary to Gray Code converter. Use Input variables: A, B, C, D and Output variables: w, x, y, z. Don't cares not allowed? (ii) Explain the working of a 4-bit carry look ahead adder with a neat diagram?	**6** **7**	2	2
	OR			
12 (b)	(i) Implement the full adder output circuit using a 3 to 8 decoder in active High output decoder circuit? (ii) Realize F (A, B, C, D) = $\sum$ (1,2,5,7,8,10,11,13,15) using a 4-to-1 MUX with A, B as selection lines and extra gates.	**6** **7**		
13 (a)	(i) Determine the equivalent states from the given state Table:1? (ii) Find the best State Assignment for the given state Table:1?	**6** **7**	3	4

Present state	Nest state		output	
	X = 0	X= 1	X= 0	X= 1
A	A	C	0	0
B	D	F	0	1
C	C	A	0	0
D	D	B	0	1
E	B	F	1	0
F	C	E	1	0

Table:1

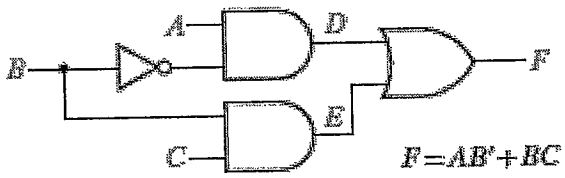


	OR			
13 (b)	(i) Design a 3-bit Ripple Up counter using JK flip-flop with a timing diagram? (ii) Draw and explain a 4-bit Universal shift register?	**6** **7**		
14 (a)	Design and implement the race free asynchronous circuit for the given reduced flow table:2?	**13**	4	4

	00	01	11	10
a	b	(a)	d	(a)
b	(b)	d	(b)	a
c	(c)	a	b	(c)
d	c	(d)	(d)	c

Table:2

	OR

14 (b)	Consider the following circuit as given in Fig:1: (i) Find all the hazards in this circuit. (ii) Redesign the circuit that is free of all hazards.  **Fig:1**	**6** **7**		
15 (a)	(i) Implement the TTL – NAND and explain the working principles? (ii) Implement NOT, AND & OR logic gates using CMOS logic design?	**6** **7**	5	2
	OR			
15 (b)	Design of sequential circuit using PLAs for the given transition table as given in Table 2?	**13**		

Present state $Q_1\ Q_2\ Q_3$	Nest state $Q_1^+\ Q_2^+\ Q_3^+$		Output Z	
	X = 0	X= 1	X= 0	X= 1
0 0 0	1 0 0	1 0 1	1	0
1 0 0	1 1 1	1 1 0	1	0
1 0 1	1 1 0	1 1 0	0	1
1 1 1	0 1 1	0 1 1	0	1
1 1 0	0 1 1	0 1 0	1	0
0 1 1	0 0 0	0 0 0	0	1
0 1 0	0 0 0	x x x	1	x
0 0 1	x x x	x x x	x	x

PART- C(1x 15=15Marks)

(Q.No.16 is compulsory)

Q.No.	Questions	Marks	CO	BL
16.	Design a state diagram (Moore model) for the given synchronous sequential circuit characteristic equation using JK flip flop? $J_A = B$ $K_A = B\,x'$ $J_B = x'$ $K_B = A'\,x + A\,x'$	**15**	3	5